What is claimed is:

1. A method for fabricating a semiconductor integrated circuit microelectronic fabrication comprising:

providing a first semiconductor substrate;

forming over the first semiconductor substrate at least one microelectronic device to form from the first semiconductor substrate a partially fabricated semiconductor integrated circuit microelectronic fabrication;

providing a second substrate;

forming over the second substrate, in inverted order, a dielectric isolated metallization pattern intended to mate with the partially fabricated semiconductor integrated circuit microelectronic fabrication; and

laminating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the second substrate to mate the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern to thus form a laminated completely fabricated semiconductor integrated circuit microelectronic fabrication.

2. The method of claim 1 wherein the microelectronic device is selected from the group consisting of resistors, transistors, diodes and capacitors.

3. The method of claim 1 wherein the second substrate is selected from the group consisting of conductor substrates, semiconductor substrates, dielectric substrates and aggregates thereof.

4. The method of claim 1 wherein the second substrate is a second semiconductor substrate.

5. The method of claim 1 wherein the first semiconductor substrate is thicker than the second substrate.

6. The method of claim 1 wherein the dielectric isolated metallization pattern comprises a plurality of laminated patterned conductor layers.

7. The method of claim 6 wherein each laminated patterned conductor layer within the plurality of laminated patterned conductor layers is formed to a thickness of from about 3000 to about 6000 angstroms.

8. The method of claim 1 wherein the mating of the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern formed over the second substrate is undertaken while employing a laminating method selected from the group consisting of thermally assisted laminating methods and pressure assisted laminating methods.

9. The method of claim 1 further comprising removing from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication the second substrate.

10. The method of claim 9 wherein the second substrate is removed from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication employing a method selected from the group consisting of etch methods, milling methods and polish methods.

11. The method of claim 9 wherein the second substrate is removed from the laminated completely fabricated semiconductor integrated circuit microelectronic fabrication employing a chemical mechanical polish (CMP) planarizing method while employing the dielectric isolated metallization pattern as an etch stop layer.

12. The method of claim 1 wherein the semiconductor substrate is not thinned after forming thereover the minimum of one microelectronic device.

13. The method of claim 1 wherein the second substrate is not removed from the dielectric isolated metallization pattern prior to mating the partially fabricated semiconductor integrated circuit microelectronic fabrication with the dielectric isolated metallization pattern.